

STATUS OF THE CLAIMS

The status of the claims of the present application stands as follows:

Claim 1-17: (Canceled)

18. (Currently amended) A device according to claim 19, further comprising a first hardmask remnant located substantially only between said second spacer and said upper surface of said source and a second hardmask remnant located between said third spacer and said upper surface of said drain portion.

19. (Currently amended) A device according to claim 17, ~~wherein each of said source portion and said drain portion includes an upper surface having a width perpendicular to said length, each of said finFETs further comprising, comprising:~~

an integrated circuit formed on a substrate and comprising a plurality of FETs wherein at least some of said plurality of FETs are finFETs each comprising:

- a) a fin having a source portion, a drain portion and a channel portion extending between said source portion and said drain portion, said fin having a base portion disposed on said substrate, each of said source portion and said drain portion having an upper surface;
- b) a first spacer formed adjacent said base portion;
- ac) a gate located at said channel portion;
- bd) a first reentrant corner between said upper surface of said source portion and said gate;
- ee) a second reentrant corner between said upper surface of said drain portion and said gate;
- el) a second spacer proximate said first reentrant corner and having a length extending along said gate substantially equal to said width of said source portion; and
- eg) a third spacer proximate said second reentrant corner and having a length extending along said gate substantially equal to said width of said drain portion.

20. (Currently amended) A device according to claim ~~17~~19, wherein said first spacer comprises silicon dioxide.

21. **(Currently amended)** A device according to claim 17~~19~~, wherein said substrate comprises an undercut region beneath at least a portion of said fin, said undercut region containing at least a portion of said first spacer.
22. **(Currently amended)** An integrated circuit, comprising:
- a) a substrate; and
 - b) a plurality of FETs formed on said substrate, wherein at least some of said plurality of FETs are finFETs each comprising:
 - i) ~~a fin having that includes a source portion having a base disposed on said substrate and further includes: a drain portion and a channel portion extending between said source portion and said drain portion, said fin having a base portion attached to said substrate; and~~
 - ii) a first spacer formed at least adjacent said base portion the entire said base portion of said source.
23. **(Currently amended)** An integrated circuit according to claim 22, wherein each of said source ~~portion~~ and said drain ~~portion~~ includes an upper surface having a width perpendicular to said length, each of said finFETs further comprising:
- a) a gate located at said channel ~~portion~~;
 - b) a first reentrant corner between said upper surface of said source ~~portion~~ and said gate;
 - c) a second reentrant corner between said upper surface of said drain ~~portion~~ and said gate;
 - d) a second spacer proximate said first reentrant corner ~~and having a length extending along said gate substantially equal to said width of said source portion; and~~
 - e) a third spacer proximate said second reentrant corner ~~and having a length extending along said gate substantially equal to said width of said drain portion.~~
24. **(Previously presented)** An integrated circuit according to claim 23, further comprising a first hardmask remnant located between said second spacer and said upper surface of said source and a second hardmask remnant located between said third spacer and said upper surface of said drain.
25. **(Previously presented)** An integrated circuit according to claim 22, wherein said first spacer comprises silicon dioxide.

26. (Previously presented) An integrated circuit according to claim 22, wherein said substrate comprises an undercut region beneath at least a portion of said fin, said undercut region containing at least a portion of said first spacer.

27. (Currently amended) A finFET formed on a substrate, comprising:

- a) a fin having a source ~~portion~~, a drain ~~portion~~ and ~~and~~ a channel ~~portion~~ extending between said source ~~portion~~ and said drain ~~portion~~, said fin having a base ~~portion~~ attached to the substrate; and
- ~~b) a first spacer formed adjacent said base portion, said fin having a length extending from, and including, said source and said drain, and each of said source and said drain including an upper surface having a width;~~
- b) a gate located at said channel;
- c) a first reentrant corner between said upper surface of said source and said gate;
- d) a second reentrant corner between said upper surface of said drain and said gate;
- c) a first spacer proximate said first reentrant corner and having a length extending along said gate substantially equal to said width of said source immediately adjacent said gate; and
- f) a second spacer proximate said second reentrant corner and having a length extending along said gate substantially equal to said width of said drain immediately adjacent said gate.

28. (Currently amended) A finFET according to claim 27, wherein each of said source ~~portion~~ and said drain ~~portion~~ includes an upper surface having a width perpendicular to said length; ~~base attached to the substrate~~, the finFET further comprising:

- a) a gate located at said channel ~~portion~~ third spacer formed adjacent the base of said source;
- ~~b) a first reentrant corner between said upper surface of said source portion and said gate;~~
- ~~c) a second reentrant corner between said upper surface of said drain portion and said gate;~~
- d) ~~a second spacer proximate said first reentrant corner and having a length extending along said gate substantially equal to said width of said source portion; and~~
- e) ~~a third spacer proximate said second reentrant corner and having a length extending along said gate substantially equal to said width of said drain portion.~~

29. **(Currently amended)** A finFET according to claim 28~~27~~, further comprising a first hardmask remnant located substantially only between said ~~second-first~~ spacer and said upper surface of said source and a second hardmask remnant located substantially only between said ~~third-second~~ spacer and said upper surface of said drain.
30. **(Previously presented)** A finFET according to claim 27, wherein said first spacer comprises silicon dioxide.
31. **(Currently amended)** A finFET according to claim 27, wherein the substrate comprises an undercut region beneath at least a said base portion of said ~~fin~~source, the undercut region containing at least a portion of said first spacer portion.

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